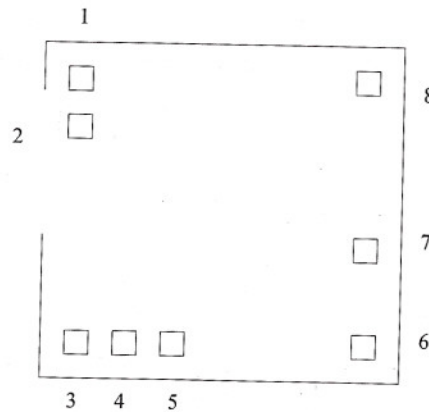




# Sierra Components, Inc.

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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**Top Material:**  
**Backside Material:**  
**Bond Pad Size:**  
**Backside Potential:**  
**Mask Ref:**

**APPROVED BY:MG**

**DIE SIZE :41x46**

**DATE: 1/20/09**

**MFG:Maxim**

**THICKNESS:**

**P/N:ICM7555**